DUAL GATE LAYOUT FOR THIN FILM TRANSISTOR

ABSTRACT

A dual gate layout of a thin film transistor of liquid crystal display to alleviate dark current leakage is disclosed. The layout comprises (1) a polysilicon on a substrate having a L-shaped or a snake shaped from top-view, which has a heavily doped source region, a first lightly doped region, a first gate channel, a second lightly doped region, a second gate channel, a third lightly doped region and a heavily doped drain region formed in order therein; (2) a gate oxide layer formed on the polysilicon layer and the substrate, (3) a gate metal layer then formed on the gate oxide layer having a scanning line and an extension portion with a L-shaped or an I-shaped. The gate metal intersects with the polysilicon layer thereto define the forgoing gate channels. Among of gate channels, at least one is along the signal line, which is connected to the source region through a source contact.